# FA7622CP(E)

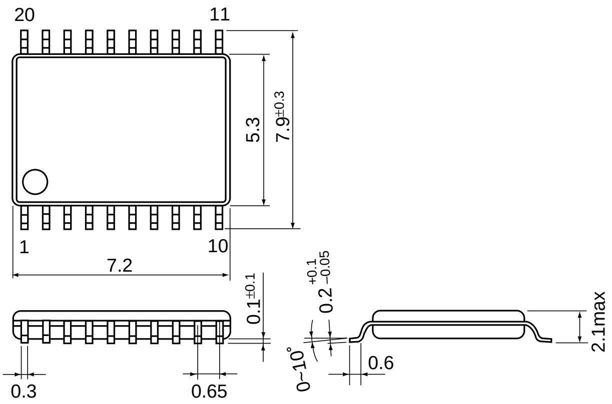
## ■ Description
The FA7622CP(E) is a DC-DC converter IC that can directly drive a power MOSFET. This IC has all the necessary protection functions for a power MOSFET. It is optimum for a portable equipment power supply which uses low-voltage input to output comparably large power.

## ■ Features
- Drive circuit for connecting a power MOSFET (Io = ±600mA)
- Built-in voltage step-up circuit to drive a power MOSFET gate: A converter circuit requires only an N-channel power MOSFET.
- Dual control circuit
- Overcurrent limiting circuit
- Overload cutoff circuit with timer and latch circuit
- ON/OFF control pin
- Wide operating range: 3.6 to 28V
- High-frequency operation: up to 1MHz
- 20-pin package (DIP/SSOP)

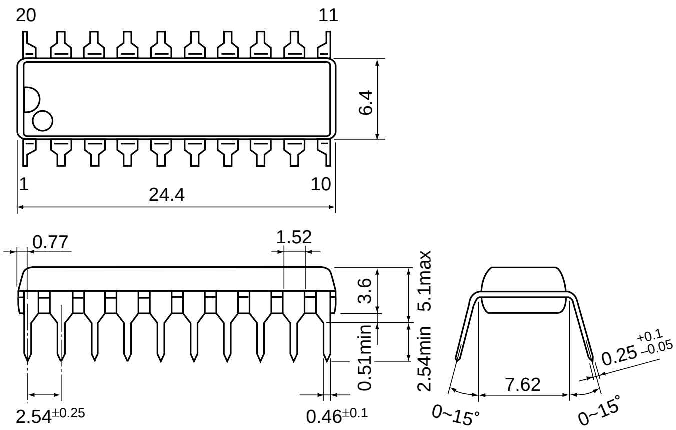
## ■ Applications
- Battery power supply for portable equipment

## ■ Dimensions, mm

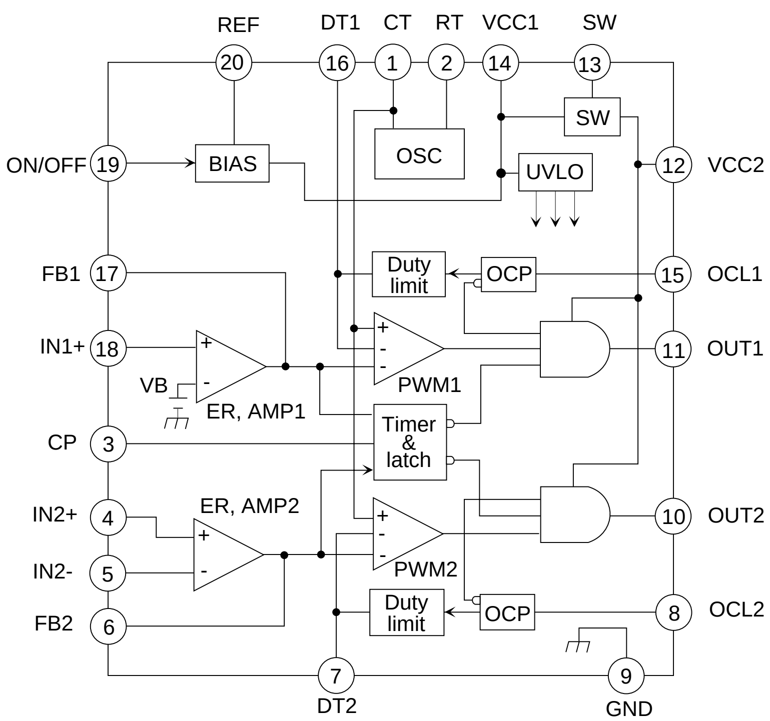
### ● SSOP-20




### ● DIP-20




## ■ Block diagram




| Pin No. | Pin symbol | Description |
|---|---|---|
| 1 | CT | Oscillator timing capacitor |
| 2 | RT | Oscillator timing resistor |
| 3 | CP | Timer and latch circuit |
| 4 | IN2+ | Non-inverting input to error amplifier |
| 5 | IN2- | Inverting input to error amplifier |
| 6 | FB2 | Error amplifier output |
| 7 | DT2 | Dead time adjustment |
| 8 | OCL2 | Overcurrent limiting circuit 2 |
| 9 | GND | Ground |
| 10 | OUT2 | CH.2 output |
| 11 | OUT1 | CH.1 output |
| 12 | VCC2 | Power supply 2 |
| 13 | SW | Switch for boost circuit |
| 14 | VCC1 | Power supply 1 |
| 15 | OCL1 | Overcurrent limiting circuit 1 |
| 16 | DT1 | Dead time adjustment |
| 17 | FB1 | Error amplifier output |
| 18 | IN1+ | Non-inverting input to error amplifier |
| 19 | ON/OFF | Output ON/OFF control |
| 20 | REF | Reference voltage output |

## ■ Absolute maximum ratings

| Item | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | Voltage boost circuit not used | $V_{CC1}$ | 28 | V |
| | Voltage boost circuit used | $V_{CC1}$ | 20 | V |
| Supply voltage | | $V_{CC2}$ | 28 | V |
| ON/OFF pin voltage | | $V_{ON/OFF}$ | –0.3 to +7 | V |
| Out pin output current | | $I_{OUT}$ | ±600 | mA |
| Total power dissipation | | $P_d$ | 650 | mW |
| Junction temperature | | $T_j$ | 125 | °C |
| Operating temperature | | $T_{opr}$ | –30 to +85 | °C |
| Storage temperature | | $T_{stg}$ | –40 to +150 | °C |

## ■ Recommended operating conditions

| Item | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | Voltage boost circuit not used | $V_{CC1}$ | 3.6 | 26 | V |
| | Voltage boost circuit used | $V_{CC1}$ | 3.6 | 18 | V |
| Feedback resistance | | $R_{NF}$ | 100 | | kΩ |
| Timing capacitance | | $C_T$ | 50 | 2200 | pF |
| Timing resistance | | $R_T$ | 24 | 100 | kΩ |
| Oscillation frequency | | $f_{OSC}$ | 50 | 1000 | kHz |

## ■ Electrical characteristics (Ta = 25°C, $V_{CC}$ = 6V, $R_T$ = 36kΩ, $C_T$ = 180pF)

### Reference voltage section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{REF}$ | $I_{OR}$ = 1mA | 2.400 | 2.475 | 2.550 | V |
| Line regulation | $L_{INE}$ | $V_{CC}$ = 3.6 to 26V, $I_{OR}$ = 1mA | | 5 | 15 | mV |
| Load regulation | $L_{OAD}$ | $I_{OR}$ = 0.1 to 1mA | | 2 | | mV |
| Output voltage variation due to temperature change | $V_{TC1}$ | Ta = –30 to +25°C | –1 | | 1 | % |
| | $V_{TC2}$ | Ta = +25 to +85°C | –1 | | 1 | % |

### Oscillator section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{OSC}$ | $C_T$ = 180pF, $R_T$ = 36kΩ | 100 | 110 | 120 | kHz |
| Frequency variation 1 (due to supply voltage change) | $f_{dV}$ | $V_{CC}$ = 3.6 to 26V | | 1 | | % |
| Frequency variation 2 (due to temperature change) | $f_{dT}$ | Ta = –30 to +25°C | | 5 | | % |

### Error amplifier section (ch. 1)

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Reference voltage | $V_B$ | | 0.832 | 0.858 | 0.884 | V |
| Input bias current | $I_B$ | | | 5 | 100 | nA |
| Open-loop voltage gain | $A_{VO}$ | | | 40 | | dB |
| Unity-gain bandwidth | $f_T$ | | | 1.0 | | MHz |
| Maximum output voltage | $V_{OH}$ | No load | 1.8 | | | V |
| | $V_{OL}$ | No load | | | 300 | mV |
| Output source current | $I_{OH}$ | $V_{OH}$ = 0V | 30 | 60 | 90 | μA |

### Error amplifier section (ch. 2)

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IO}$ | | | 2 | 10 | mV |
| Input bias current | $I_B$ | | | 5 | 100 | nA |
| Common-mode input voltage | $V_{COM}$ | | 0 | | 1.0 | V |
| Open-loop voltage gain | $A_{VO}$ | | 70 | | | dB |
| Unity-gain bandwidth | $f_T$ | | | 1.0 | | MHz |
| Maximum output voltage | $V_{OH}$ | No load | 1.8 | | | V |
| | $V_{OL}$ | No load | | | 300 | mV |
| Output source current | $I_{OH}$ | $V_{OH}$ = 0V | 40 | 80 | 120 | μA |

### Pulse width modulation circuit section ( FB1, FB2 pin )

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input threshold voltage | $V_{THO}$ | Duty cycle = 0% | | 1.6 | 1.8 | V |
| Input threshold voltage | $V_{THI}$ | Duty cycle = 100% | 0.8 | 1.0 | | V |

### Dead time adjustment circuit section ( DT1, DT2 pin )

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input threshold voltage | $V_{TH0}$ | Duty cycle = 0% | | 1.6 | 1.8 | V |
| Input threshold voltage | $V_{TH1}$ | Duty cycle = 100% | 0.8 | 1.0 | | V |
| Standby voltage | $V_{STR}$ | DT1, DT2 pin open | 1.8 | | | V |

### Overcurrent limiting circuit section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input threshold voltage | $V_{THOC}$ | | 180 | 210 | 240 | mV |
| Hysteresis voltage | $V_{HYOC}$ | | | 40 | | mV |
| Input bias current | $I_{OC}$ | | | 50 | 100 | μA |
| Delay in OCL | $t_{doc}$ | Overdriving: 50mV | | 120 | | ns |

### Timer and latch circuit section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Latch-mode threshold voltage | $V_{THCP}$ | | 1.00 | 1.25 | 1.50 | V |
| Input bias current | $I_{INCP}$ | $V_{CP}$ = 1.5V, $V_{FB}$ = 0.3V | | | 1 | μA |
| CP pin voltage / LOW | $V_{SATC}$ | $I_{CP}$ = 20 μA, $V_{FB}$ = 1.0V | | | 300 | mV |

### Output ON/OFF control circuit section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| OFF-to-ON threshold voltage | $V_{THON}$ | | | | 3.0 | V |
| ON-to-OFF threshold voltage | $V_{TH\ OFF}$ | | 0.60 | | | V |
| Input bias current | $I_{IN}$ | $V_{IN}$ = 3V | | 180 | | μA |

### Undervoltage lock-out circuit section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| OFF-to-ON threshold voltage | $V_{CCON}$ | | 2.80 | 3.00 | 3.20 | V |
| ON-to-OFF threshold voltage | $V_{CCOF}$ | | | 2.90 | | V |
| Voltage hysteresis | $V_{HYS}$ | | | 0.10 | | V |

### Output section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Saturation voltage (H level) | $V_{SAT+}$ | $I_O$ = –50mA | | 1.50 | 2.00 | V |
| Saturation voltage (L level) | $V_{SAT-}$ | $I_O$ = 50mA | | 1.70 | 2.20 | V |

### Voltage step-up circuit section

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{OUP}$ | L=330μH, C=1μF, No load | 10.5 | 12.5 | 14.0 | V |

### Overall device

| Item | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Stand-by supply current | $I_{CCST}$ | Out pin open | | 0.1 | 10 | μA |
| Operating $V_{CC1}$ current | $I_{CC1}$ | Normal operation | | 3.8 | 5.5 | mA |
| Operating $V_{CC2}$ current | $I_{CC2}$ | Normal operation $V_{CC2}$=12V<br>OUT1, OUT2 open<br>Duty cycle=50% | | 1.5 | 2.2 | mA |

## ■ Description of each circuit

### 1. Oscillator section

This section charges and discharges an external capacitor $C_T$. The charge current is determined by the external resistor $R_T$ connected to the IC. By charging and discharging the capacitor, this section provides a 1.0 to 1.6V triangle wave at the CT pin. The oscillation frequency can be set between 50kHz to 1MHz. The frequency can be calculated approximately as follows:

$$f_{OSC}\ (kHz) = \frac{7.1 \cdot 10^5}{R_T\ (k\Omega) \cdot C_T\ (pF)} \quad \text{.....................} \ (1)$$

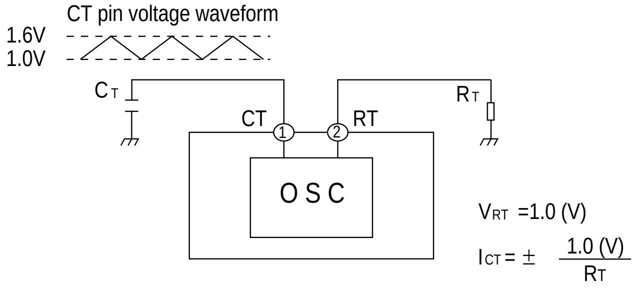



**Fig. 1 Oscillator**

### 2. Error amplifier section

**Error amplifier ①**

As Fig. 3 shows, the inverting input of the error amplifier is connected to the $V_B$ reference voltage (0.858V typ.). The non-inverting input IN1+ and output FB1 connect to external terminals.

During ordinary operation, the IN1+ terminal voltage is almost equal to $V_B$. The power-supply output $V_{OUTA}$ can be determined as follows:

$$V_{OUTA} = \frac{R_1 + R_2}{R_2} \cdot V_B \quad \text{...................................} \ (2)$$

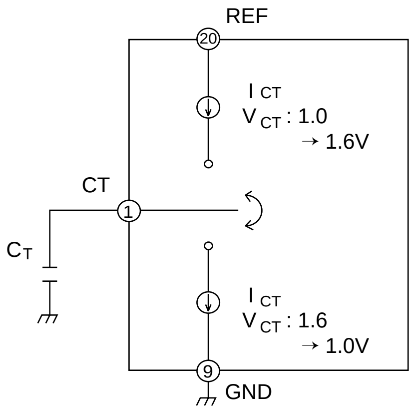



**Fig. 2**

The DC gain of the error amplifier is 40dB (typ.), regardless of external parts connected to the IC. Correct the phase by connecting capacitor $C_1$ between the $V_{OUTA}$ and FB1 pins.

**Error amplifier ②**

**• Voltage step-up or step-down chopper circuit**

As Fig. 4 shows, the non-inverting input IN2+, inverting input IN2–, and output FB2 of the error amplifier are connected to external terminals.

The feedback voltage $V_{OUTB}$ to the IN2+ pin can be determined as follows:

$$V_{OUTB} = \frac{(R_3 + R_4) \cdot R_6}{R_4 \cdot (R_5 + R_6)} \cdot V_{REF} \quad \text{.......................} \ (3)$$

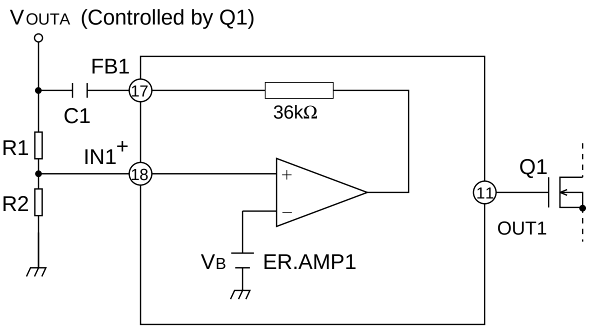



**Fig. 3**

The DC gain $A_V$ from the $V_{OUTB}$ to FB2 pin is 70dB (min), when $R_7$ is not connected.

When $R_7$ is connected, the $A_V$ can be determined as follows:

$$A_V = \frac{R_4}{R_3 + R_4} \cdot \left(1 + \frac{R_7 \cdot (R_5 + R_6)}{R_5 \cdot R_6}\right) \quad \text{...........} \ (4)$$

To correct the phase, connect the resistor R8 and capacitor C2 in series between the IN2– and FB2 pins.

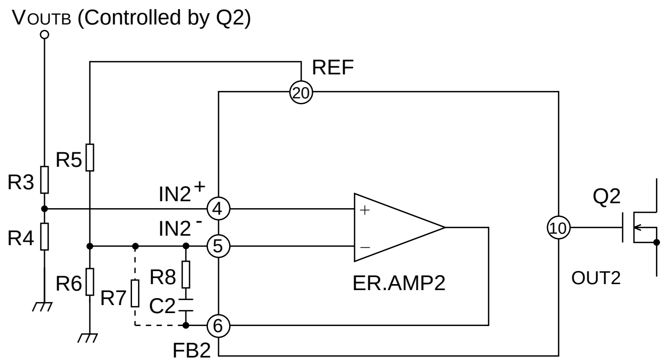



**Fig. 4**

**• Inverting chopper circuit**

According to the circuit shown in Fig. 5, the power output voltage $V_{OUTB}$ can be determined as follows:

$$V_{OUTB} = -\frac{R_{11}}{R_{10}} \cdot V_{REF} \quad \text{.............................} (5)$$

The $A_V$ between the $V_{OUTB}$ and FB2 pins can be determined as follows:

$$A_V + \frac{-R_{11}}{R_{12}} \quad \text{................................................} (6)$$

To correct the phase, connect the resistor $R_{13}$ and capacitor $C_3$ in series between the IN2– and FB2 pins.
By using this circuit, invert the output polarity of OUT2 with an external transistor to drive a P-channel MOSFET (or PNP transistor).

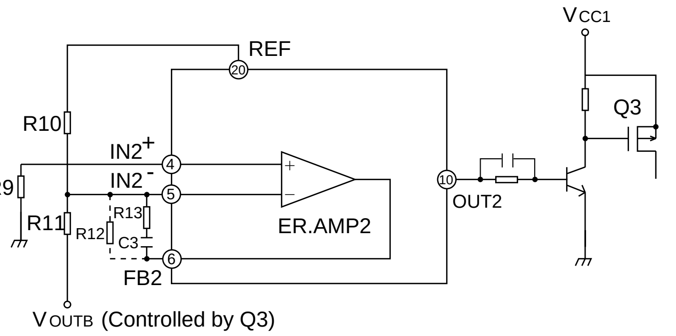



**Fig. 5**

### 3. PWM comparator section

As Fig. 6 shows, a PWM comparator has three input terminals. PWM comparator 1 determines the duty cycle of the output from the OUT1 pin. This comparator compares the $C_T$ oscillator Voltage (Pin 1) with the FB1 voltage (Pin 17) or the DT1 voltage (Pin 16), whichever is greater. When the highest of these voltages is lower than the $C_T$ voltage, the PWM output is high. When it is higher than $C_T$, the PWM output is low.
PWM comparator 2 determines the duty cycle of the output from the OUT2 pin. To determine the PWM output, this comparator compares the $C_T$ oscillator voltage (Pin 1) with the FB2 voltage (Pin 6) or the DT2 voltage (Pin 7) whichever is higher.
During ordinary operation, the OUT1 and OUT2 pin voltages have the same polarity as the output from each comparator.
When the power supply is turned on, the pulse width gradually increases. The time constant for soft-start is determined by the external resistor and capacitor across pins 16 and 7. In Figures 7 and 8, the time ts required for the pulse width (duty-cycle) to reach about 30% after start-up can be determined as follows:
(Units: µF for Cs and kΩ for Rs, Rs1, and Rs2)

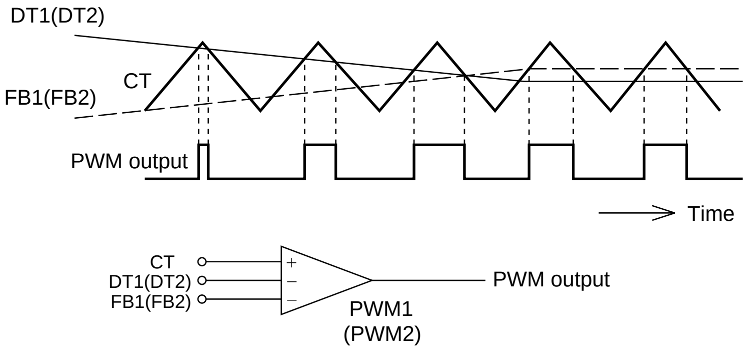



**Fig. 6**

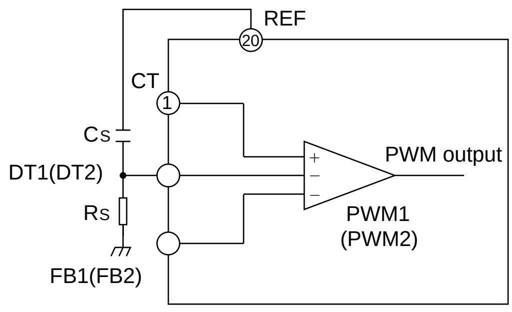



**Fig. 7**

Fig.7:

$$ts\ (ms) = 0.54C_S \cdot R_S \quad \text{................................} (7)$$

Fig.8:

$$ts\ (ms) = CS\left(\frac{R_{S1} \cdot R_{S2}}{R_{S1} + R_{S2}}\right) \cdot \ln\left(\frac{R_{S1}}{0.417R_{S1} - 0.583\ R_{S2}}\right) \text{......} (8)$$

Where, $R_{S1}$ / $R_{S2}$ > 0.716

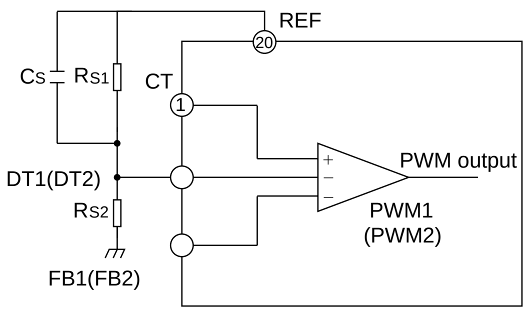



**Fig. 8**

Please connect enough large capacitance between REF and GND pins in order to prevent irregular output pulse caused by minus voltage at DT1 or DT2 pin when IC is shut down.

### 4. Timer and latch circuit for overload protection

Figure 9 shows the timer and latch circuit for overload protection and Fig. 10 shows its timing during an overload.
If the power supply output decreases due to an overload, the error amplifier output decreases. If the voltage decreases to less than 0.3V, the switch that clamps the CP pin voltage to the ground disconnects. This charges capacitor Cp from the REF pin through the resistor Rcp and the CP pin voltage increases. When the voltage reaches 1.25V, OUT1 (OUT2) voltage is clamped to ground.
The N-channel MOSFET (or NPN transistor) connected to the OUT1 (or OUT2) is turned OFF and cuts off the power supply.
The time $t_L$ from when the circuit is overloaded until the power supply is cut off can be determined as follows:

$t_L$ (ms) = 0.67$C_P$ (μF) • $R_{CP}$ (kΩ) .................(9)

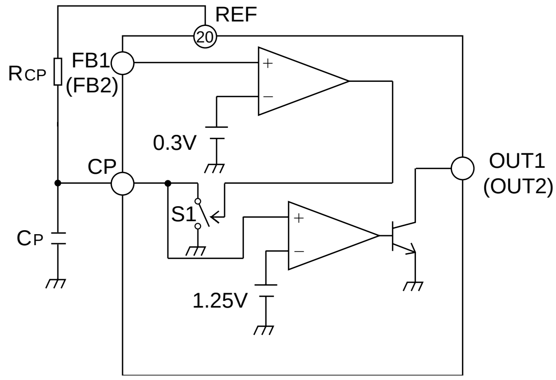



Fig. 9

### 5. Overcurrent limiting circuit

This is a pulse-by-pulse overcurrent limiting circuit which detects and limits the peak of each drain current pulse from the main switching transistor (MOSFET).
Figure 11 shows the overcurrent limiting circuit and Fig. 12 shows its timing.
This circuit detects a drain current with a voltage sampling resistor Rs. If a voltage lower than the $V_{CC1}$ pin voltage by 210mV or more is input to OCL1 (OCL2), the OUT1 (OUT2) is clamped to ground. At the same time, DT1 (DT2) is raised to the reference voltage $V_{REF}$. (This reduces the duty-cycle to 0%)
This circuit has hysteresis to prevent noise from causing malfunction.
The Rs voltage which is propotional to drain current is limited to 210mV (typ.) and released at 170mV (typ).

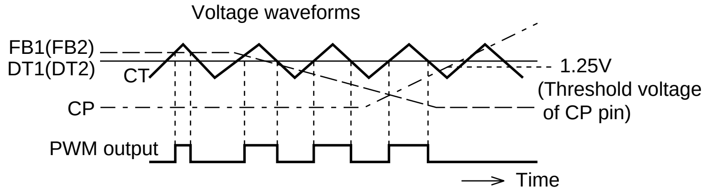



Fig. 10

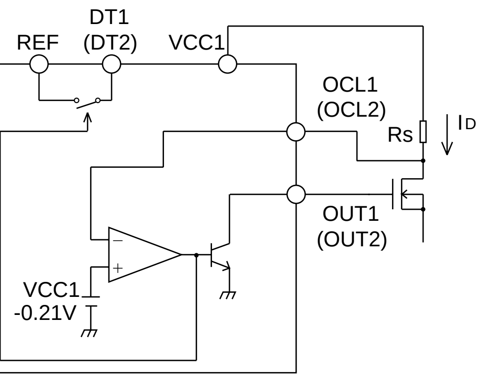



Fig. 11

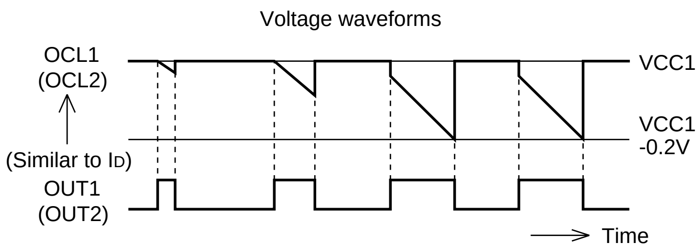



Fig. 12

### 6. IC ON/OFF control circuit

This control circuit turns the entire IC ON or OFF by an external signal using an ON/OFF control pin to limit the IC's current consumption to 10µA or less.
Figure 13 shows the IC ON/OFF control circuit and Fig. 14 shows its timing.
To turn the IC OFF, this circuit clamps OUT1 (OUT2) to ground when the ON/OFF pin voltage is controlled to less than 0.60V. The internal bias current is cut off to turn off the switching transistor.
To turn the IC ON, raise the ON/OFF pin voltage immediately to 3.0V or more to charge the soft-start capacitor gradually.

### 7. Voltage boost circuit

By using the circuit shown in Fig. 15, this IC generates a voltage 6.5V (typ.) higher than the VCC1 input voltage at the VCC2 pin. This circuit allows the IC to drive MOSFET gates directly. With this circuit, the IC can drive a low-level side N-channel MOSFET at 3.6 to 18V as VCC1 (not possible with conventional ICs). In addition, an N-channel MOSFET can be used on the high-level side of a buck chopper. In Fig. 15, the inductor (L) is about 100µH or more and the capacitor (Cup) should be greater than about 0.1µF.
If voltage boost is not necessary, connect the VCC1 and VCC2 pins directly, and SW pin must be opened.

### 8. Undervoltage lock-out circuit

This circuit prevents a malfunction at a low supply voltage. When the supply voltage VCC1 rises and reaches 3.0V, this circuit is activated. When VCC1 drops below 2.9V, this circuit clamps OUT1 (OUT2) to ground. The CP pin voltage is reset to low by means of cutting off a power supply input.

### 9. Output circuit

As Fig. 17 shows, OUT1 and OUT2 with a totempole structure can drive a MOSFET.
Since both the maximum output source and sink currents are 600mA, a MOSFET can be switched at high speed.

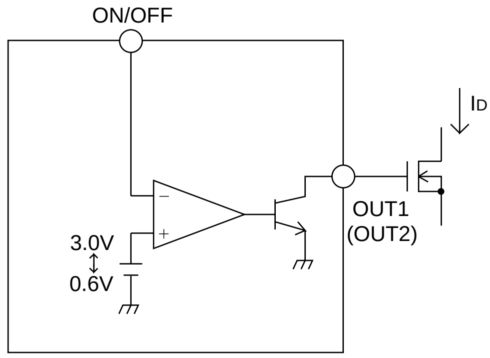



**Fig. 13**

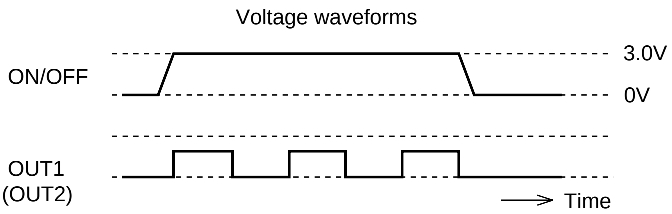



**Fig. 14 Control of output**

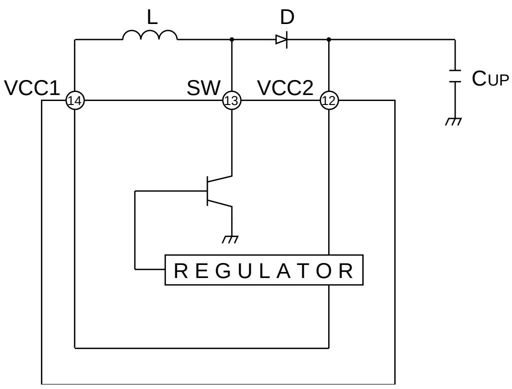



**Fig. 15**

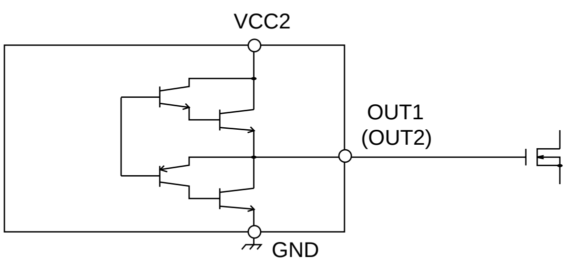
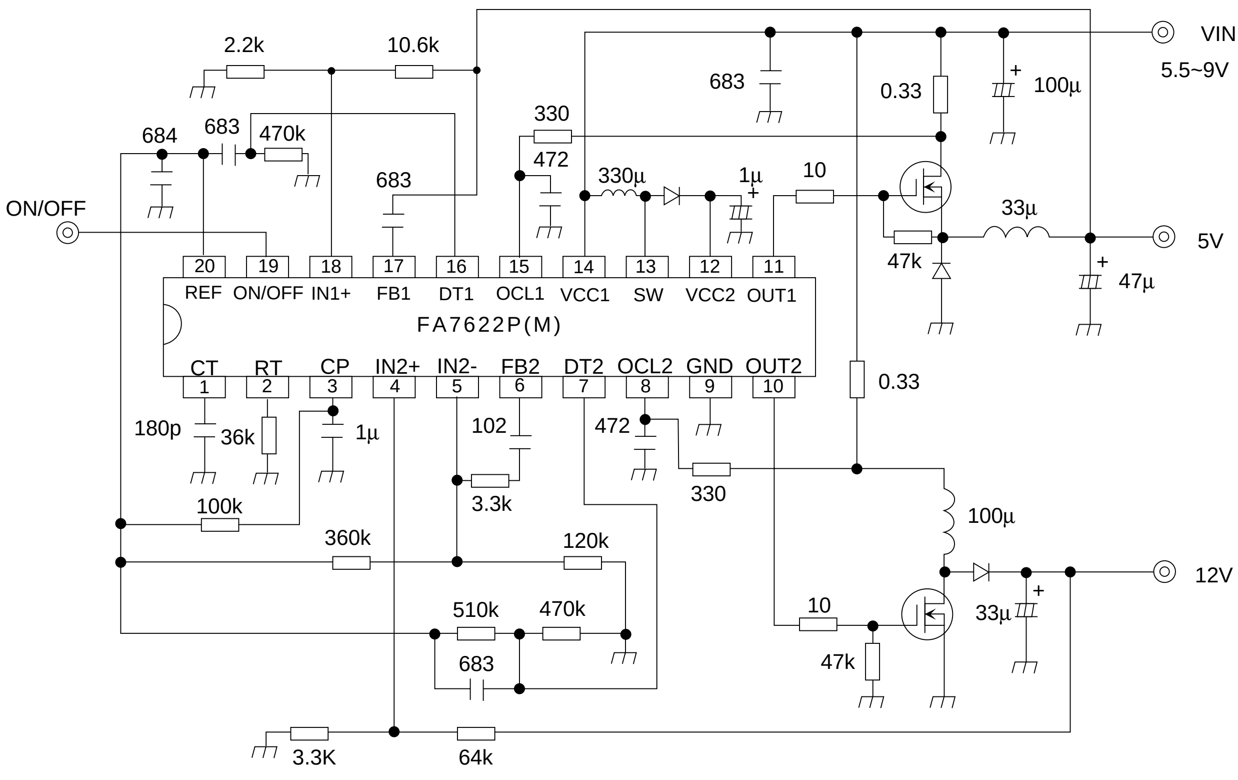



**Fig. 16**

## ■ Application circuit




*Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.*